UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/832,605	04/11/2001	Rama Divakaruni	FIS920000337US1 (14114)	1873

7590 03/14/2003

Richard L. Catania, Esq.
Scully, Scott, Murphy & Presser
400 Garden City Plaza
Garden City, NY 11530

EXAMINER	
LOKE, STEVEN HO YIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/832,605	DIVAKARUNI ET AL	
	Examiner	Art Unit	
	Steven Loke	2811	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondenc address* --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *6-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-5* is/are rejected.

7)☒ Claim(s) *2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

1. Claim 1 is objected to because of the following informalities: line 9, the phrase "a body contact:" is unclear. The paragraph extending between pages 3 and 4 discloses a body region [19] is isolated from the capacitor [22] by an intact collar oxide. Therefore, it is believed that the collar oxide region is used to electrically isolating a body region from the underlying capacitor in claim 1. Appropriate correction is required.

2. Claim 2 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 2 discloses the intermediate structure of the invention. Specifically, claim 2 discloses the TTO layer is additionally formed on sidewalls of the DRAM cell array and the horizontal surface in fig. 2(b). However, claim 1, the parent claim of claim 2, is directed to a final structure of the invention in fig. 2(h).

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 and 3-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Gruening et al. (U.S. patent no. 6,437,381).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In regards to claim 1, Gruening et al. show all the elements of the claimed invention in fig. 15. It is a memory cell in a DRAM (col. 9, lines 3-22), comprising: a deep trench region [200] having a vertical MOSFET (the MOSFET is located in the top portion of the trench which includes a gate oxide [160], source and drain regions [18, 62], and a gate electrode (not shown in the figure, but it is disclosed in the prior art (element [48] in fig. 12, see also col. 7, lines 31-32) formed on the top of the gate oxide [160]) and an underlying capacitor [34-36] formed therein that are in electrical contact to each other through at least one buried-strap outdiffusion region [62] which is present within a portion of a wall of the deep trench; the memory cell having a deep trench conductor [36] forming an electrode of the underlying capacitor and a collar oxide region [130] formed in a portion of the deep trench; the collar oxide region formed on a remaining wall portion of the deep trench not containing the buried-strap outdiffusion region [62] for electrically isolating a body region [50] from said underlying capacitor [34-36]; and a trench top oxide layer [160] formed on a horizontal surface of the memory cell for isolating the deep trench conductor [36] forming an electrode of the underlying capacitor [34-36] and the buried-strap outdiffusion [62] from a gate conductor region (the gate

electrode that formed on the top of the gate oxide [160]); an underlying nitride layer (a bottom portion of layer [1250]) formed between a top of the deep trench conductor [36] and the buried-strap outdiffusion region [62] and underlying the trench top oxide [160].

It is inherent that the underlying the nitride layer is used to eliminate a possibility of the trench top oxide layer dielectric breakdown between the gate conductor and the electrode [36] of the underlying capacitor.

Since Gruening et al. disclose their invention relates to vertical transistor structures in the trench capacitors of DRAM (col. 1, lines 7-10), a plurality of memory cells each having a structure of fig. 15 would be formed in the semiconductor substrate. It is inherent that the memory cells of Gruening et al. are formed in a DRAM cell array which are arranged in rows and columns because it is well known in the art that memory cells in a DRAM cell array are arranged in rows and columns.

In regards to claim 3, Gruening et al. further disclose a sacrificial oxide layer [14] formed underneath the nitride layer [1250]. It is inherent that the oxide layer [14] further eliminates a possibility of trench top oxide layer [160] dielectric breakdown between the gate conductor region and the deep trench conductor [36].

In regards to claim 4, Gruening et al. further disclose the nitride layer [1250] is deposited to a thickness of 1.0 nm (col. 10, lines 14-15).

In regards to claim 5, Gruening et al. further disclose the vertical MOSFET includes gate dielectrics (a sidewall portion of layer [160] and a sidewall portion of layer [1250]) formed on the inner surfaces of the sidewalls of the deep trench [200]. Since Gruening et al. disclose their invention relates to vertical transistor structures in the trench

capacitors of DRAM (col. 1, lines 7-10), a plurality of memory cells each having a transistor structure of fig. 15 are formed in the semiconductor substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

sl
March 13, 2003

Steven Loke
Primary Examiner
Steven Loke